REMARKS/ARGUMENTS

The office action of June 7, 2004 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-13 remain in this application.

Claims 1-13 stand rejected under 35 U.S. C. § 102(b) as being anticipated by U.S. patent no. 5,841,711 to Watanabe. Applicants respectfully traverse this rejection.

The action alleges that Watanabe discloses all the elements of independent claim 1. Claim 1 recites, among other features, a first nonvolatile storage configured to store semiconductor chip codes of semiconductor chips; a latch circuit configured to latch an address upon receipt of an activating signal; and a first comparator circuit configured to compare a semiconductor chip code inputted from an external source with the semiconductor chip codes stored in the first storage, and output the activating signal when the inputted chip code coincides with one of the stored chip codes. To show the first nonvolatile storage and first comparator circuit recited in claim 1, the action relies on the latch flag circuit and comparator circuit 10, respectively, shown in Fig. 6 of Watanabe. As applicants understand the rejection, the latch flag circuit corresponds to any one of circuits 16_1, 16_n, 18_1, 18_m shown in Fig. 6 of Watanabe.

Contrary to the action's position, no latch flag circuit of Watanabe stores semiconductor chip codes of semiconductor chips. Rather, the latch flag circuits of Watanabe store addresses of defective memory cells. Thus, Watanabe neither teaches nor suggests a first nonvolatile storage configured to store semiconductor chip codes of semiconductor chips as recited in claim 1.

Moreover, contrary to action's contention, Watanabe does not provide any teaching or suggestion that the comparator circuit 10 is configured to compare a semiconductor chip code inputted from an external source with the semiconductor chip codes stored in the first storage. Instead, the comparator circuit 10 compares DIN the output of the QC buffer 5 with the output of the sense amplifier 8 as shown in Fig. 6 of Watanabe. The comparator circuit 10 does not even compare DIN with the any of the latch flag circuits, which the action alleges corresponds to the first nonvolatile storage recited in claim 1.

In view of the above, Watanabe clearly fails to provide a teaching or suggestion of all the elements of claim 1. For at least this reason, claim 1 is patentably distinct over Watanabe. Also,

claims 2-13, which ultimately depend from claim 1, are patentable over Watanabe for the same reasons as claim 1, and further in view of the novel and non-obvious features recited therein.

CONCLUSION

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

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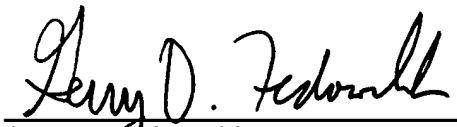
By: 

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